ORIENT

Photo coupler

Product Data Sheet

Part Number: OR-3120(B)_OR-3150(B)

Customer: ______________________

Date: ______________________

一级代理商：

深圳市弗瑞鑫电子有限公司

地址：深圳市宝安区西乡大道302号金源商务大厦B座三楼

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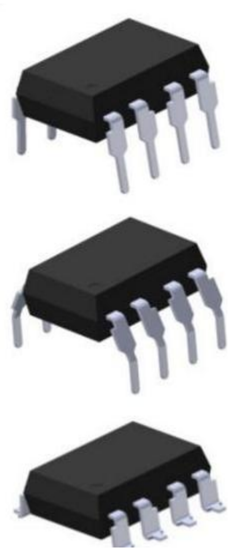


(1) 1.5A maximum peak output current for OR-3150(B),
3.0A maximum peak output current for OR-3120(B).
(2) 35-kV/µs minimum Common Mode Rejection (CMR) at V_{CM} = 1500V
(3) 1.0V maximum low level output voltage (V_{OL}) eliminates need for negative gate drive
(4) I_{CC} = 5 mA maximum supply current
(5) Under voltage lock-out protection (UVLO) with hysteresis
(6) Wide operating V_{CC} range: 15V to 35V
(7) 0.2µs maximum propagation delay
(8) ±0.1µs maximum delay between devices/channels
(9) Industrial temperature range: –40°C to 110°C
(10) Safety approval

UL approved(No.E323844)

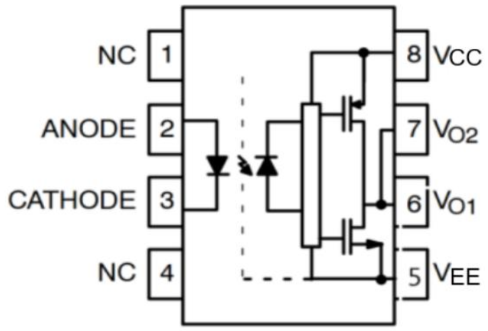
VDE approved(No.40029733)

CQC approved (No.CQC19001231254)

(11) In compliance with RoHS, REACH standards
(12) MSL Class

The OR-3120(B)/OR-3150(B) consists of an LED optically coupled to an integrated circuit with a power output stage. This optocoupler is ideally suited for driving power IGBTs and MOSFETs used in motor control inverter applications. The high operating voltage range of the output stage provides the drive voltages required by gate-controlled devices. The voltage and current supplied by this optocoupler makes it ideally suited for directly driving IGBTs with ratings up to 1200V/50A.

(1) IGBT/MOSFET gate drive
(2) AC/Brushless DC motor drives
(3) Industrial inverters
(4) Switch mode power supplies



LED	VCC – VEE "POSITIVE GOING" (TURN-ON)		VCC – VEE "NEGATIVE GOING" (TURN-OFF)	
	VCC – VEE	VO	VCC – VEE	VO
OFF	0 – 30 V	LOW	30 – 0 V	LOW
ON	0 – 11.0 V	LOW	30 – 12.0 V	HIGH
ON	11.0 – 13.5 V	TRANSITION	12.0 – 9.5 V	TRANSITION
ON	13.5 – 30 V	HIGH	9.5 – 0 V	LOW

Input	Average Forward Input Current		I_F	25	mA
	Reverse Input Voltage		V_R	5	V
Output	"High" Peak Output Current	OR-3120(B)	$I_{OH(PEAK)}$	3.0	A
		OR-3150(B)		1.5	
	"Low" Peak Output Current	OR-3120(B)	$I_{OL(PEAK)}$	3.0	A
		OR-3150(B)		1.5	
	Output Collector Power Dissipation		P_O	250	mW
Total Power Dissipation			P_T	295	mW
Total Output Supply Voltage			$V_{CC} - V_{EE}$	35	V
Total Output Supply Voltage (90)			$V_{CC} - V_{EE}$	30	V
Insulation Voltage			V_{iso}	5000	Vrms
Working Temperature			T_{opr}	-40 + 110	
Storage Temperature			T_{stg}	-55 + 125	
*2 Soldering Temperature			T_{sol}	260	

*1. Room temperature = 25 . Exceeding the maximum absolute rating can permanently damage the device. Working long hours at the maximum absolute rating can affect reliability.
*2. soldering time is 10 seconds.

Operating Temperature	T_A	-40	110	
Power Supply	$V_{CC}-V_{EE}$	15	30	V
Input Current	$IF_{(ON)}$	7	16	mA
Input Voltage(OFF)	$VF_{(OFF)}$	0	0.8	V

High Level Output Current	OR-3120	I_{OH}	1.0	2.3	2.5		$V_O = (V_{CC} – 3V)$
			2.0	—	2.5		$V_O = (V_{CC} – 6V)$
	OR-3150		0.2	—	—	A	$V_O = (V_{CC} – 0.75V)$
			1.0	—	—		$V_O = (V_{CC} – 4V)$
Low Level Output Current	OR-3120	I_{OL}	1.0	2.5	2.5		$V_O = (V_{EE} + 3V)$
			2.0	—	2.5		$V_O = (V_{EE} + 6V)$
	OR-3150		0.2	—	—	A	$V_O = (V_{EE} + 0.75V)$
			1.0	—	—		$V_O = (V_{EE} + 4V)$
High Level Output Voltage		V_{OH}	(VCC – 0.3)	(VCC – 0.1)	—	V	I_O = –100 mA
Low Level Output Voltage	OR-3120	V_{OL}	—	0.06	0.25	V	I_O = 100 mA
	OR-3150		—	0.4	1.0		
High Level Supply Current		I_{CCH}	—	1.5	3.0	mA	Output Open, I_F = 7 to 16 mA
Low Level Supply Current		I_{CCL}	—	1.6	3.0	mA	Output Open, V_F = –3.0 to +0.8V
Threshold Input Current Low to High		I_{FLH}	—	1.9	5.0	mA	I_O = 0 mA, V_O 5V
Threshold Input Voltage High to Low		V_{FHL}	0.8	—	—	V	I_O = 0 mA, V_O 5V
Input Forward Voltage		V_F	1.2	1.5	1.8	V	I_F = 10 mA
Temperature Coefficient of Forward Voltage		$\Delta V_F/\Delta T_A$	—	–1.6	—	mV/°C	I_F = 10 mA
Input Reverse Breakdown Voltage		BV_R	5	—	—	V	I_R = 10 µA
Input Capacitance		C_{IN}	—	70	—	p	

1. All typical values at T_A = 25°C and $V_{CC} – V_{EE}$ = 30V, unless otherwise noted.
2. Maximum pulse w[illegible]h = 10 µs, maximum duty cycle = 0.2%. This value is intended to allow fo[illegible]ponent tolerances for [illegible] with I_O pe[illegible] minimum = 0.5 A. See Applications section for addition[illegible]tails on [illegible]ng I_O peak.

[illegible] 50 µs, maximum duty cycle = 0.5%.

In this test, V[illegible] measured with a dc load current. When driving capacitive loads V_{OH} will approach V_{CC} as I_{OH} approaches zero amps.

Maximum pulse [illegible]h = 1 ms, maximum duty cycle = 20%.

Propagation Delay Time to High Output Level	t_{PLH}	0.05	0.11	0.20	μs	Rg=10 ,Cg=10nF, f=10kHz, Duty Cycle=50%
Propagation Delay Time to Low Output Level	t_{PHL}	0.05	0.11	0.20	μs	
Pulse Width Distortion	PWD	—	0.005	0.06	μs	
Propagation Delay Difference Between Any Two Parts	PDD ($t_{PHL} - t_{PLH}$)	–0.1	—	0.1	μs	Rg=47Ω,Cg=3nF, f=10kHz, Duty Cycle = 50%
Rise Time	t_r	—	0.05	—	μs	
Fall Time	t_f	—	0.05	—	μs	
UVLO Turn On Delay	$t_{UVLO\ ON}$	—	0.9	—	μs	V_O>5V,I_F=10mA
UVLO Turn Off Delay	$t_{UVLO\ OFF}$	—	0.8	—		V_O<5V,I_F=10mA
Output High Level Common Mode Transient Immunity	$\|CM_H\|$	35	50	—	kV/μs	T_A=25°C, I_F=10 to 16mA,
Output Low Level Common Mode Transient Immunity	$\|CM_L\|$	35	50	—	kV/μs	T_A=25°C, V_{CM}= 1500V, V_F=0V,V_{CC}=30V

1. All typical values at T_A = 25 °C and $V_{CC} - V_{EE}$ = 30 V, unless otherwise noted.
2. This load condition approximates the gate load of a 1200 V/75A IGBT.
3. Pulse Width Distortion (PWD) is defined as $|t_{PHL}-t_{PLH}|$ for any given device.
4. The difference between t_{PHL} and t_{PLH} between any two OR-3120(B) parts under the same test condition.
5. Pins 1 and 4 need to be connected to LED common.
6. Common mode transient immunity in the high state is the maximum tolerable dV_{CM}/dt of the common mode pulse, V_{CM}, to assure that the output will remain in the high state (i.e., V_O>15.0V).
7. Common mode transient immunity in a low state is the maximum tolerable dV_{CM}/dt of the common mode pulse, V_{CM}, to assure that the output will remain in a low state (i.e., V_O<1.0V).

3120(B) / 3150(B) = Part Number.

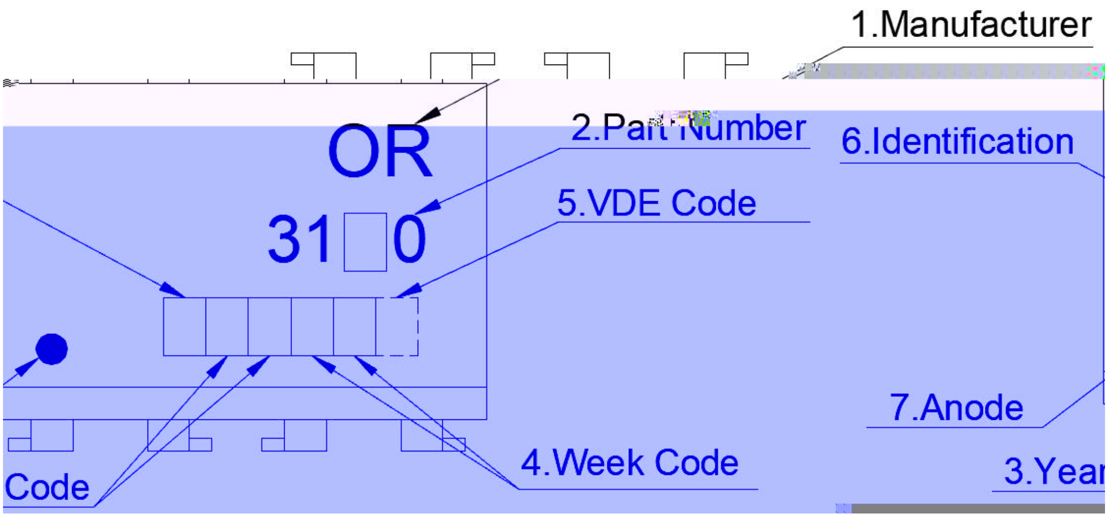
U = Lead form option (S, M or none)

Y = Tape and reel option (TA,TA1 or none).

Z = ‘V’ code for VDE safety (This options is not necessary).

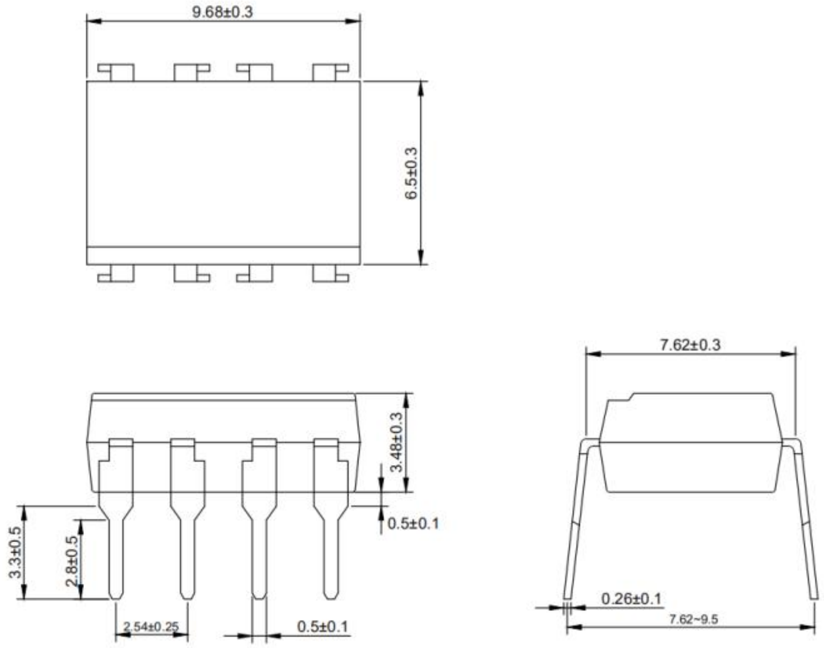
* VDE Code can be selected.

None	Standard DIP Option	45 units per tube
M	Wide lead bend (0.4 inch spacing)	45 units per tube
TA	Surface mount lead form (low profile) + TA tape & reel option	1000 units per reel
TA1	Surface mount lead form (low profile) + TA1 tape & reel option	1000 units per reel

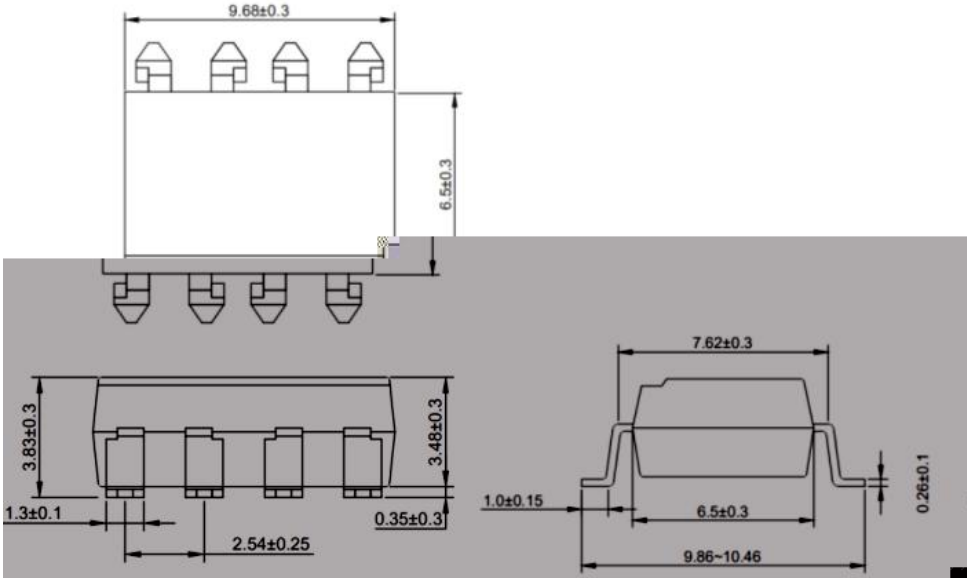


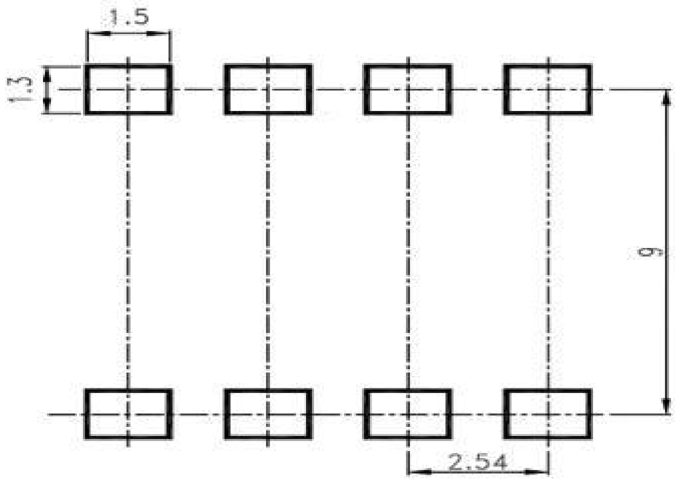
1. Manufacturer : ORIENT.
2. Part Number : 3120 or 3150.
3. Year Code □□： '21' means '2021' and so on.
4. Week Code □□： 01 represents the first week, 02 represents the second week, and so on.
5. VDE Code ⬚ (Optional)
6. Identification “B”.
7. Anode.

* VDE Mark can be selected.


9.68±0.3
6.5±0.3
7.62±0.3
3.48±0.3
0.5±0.1
3.3±0.5
2.8±0.5
2.54±0.25
0.5±0.1
0.26±0.1
7.62~9.5


9.68±0.3
6.5±0.3
7.62±0.3


9.68±0.3
6.5±0.3
3.83±0.3
3.48±0.3
1.3±0.1
0.35±0.3
2.54±0.25
7.62±0.3
1.0±0.15
6.5±0.3
0.26±0.1
9.86~10.46


1.5
1.3
9
2.54

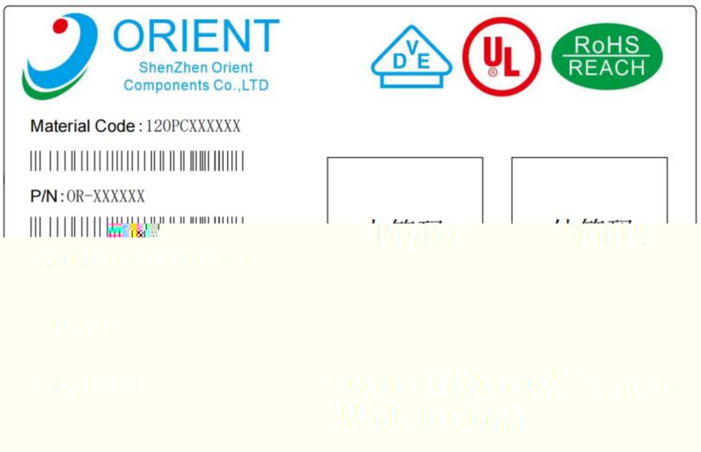
unit mm

type	symbol	Size: mm	inches
bandwidth	W	16±0.3	SP

W K

DIP Type

SOP Type

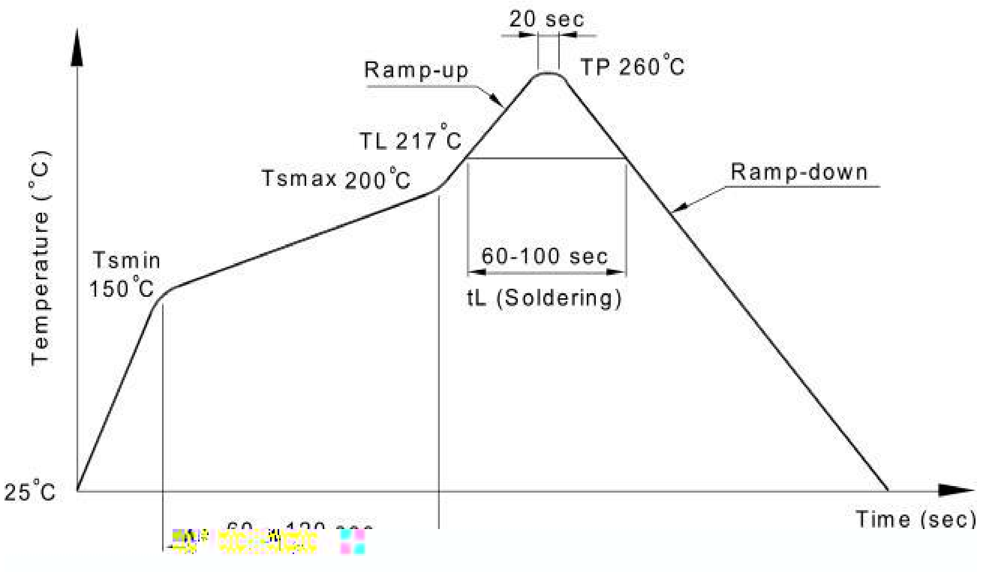


1. Material Code :Product ID.
2. P/N :Contents with "Order Information" in the specification.
3. Lot No. :Product data.
4. D/C :Product weeks.
5. Quantity :Packaging quantity.

IR Reflow soldering (JEDEC-STD-020C compliant)

Note: one solder backflow is recommended under the conditions described below in the temperature and time profile. Do not weld more than three times.

Preheat - Temperature Min (T Smin) - Temperature Max (T Smax) - Time (min to max) (ts)	150˚C 200˚C 90±30 sec
Soldering zone - Temperature (TL) - Time (t L)	217˚C 60 sec
Peak Temperature	260˚C
Peak Temperature time	20 sec
Ramp-up rate	3˚C / sec max.
Ramp-down rate from peak temperature	3~6˚C / sec
Reflow times	≤3



Wave soldering (JEDEC22A111 compliant)

Figure 1: V_{OH} vs. Temperature

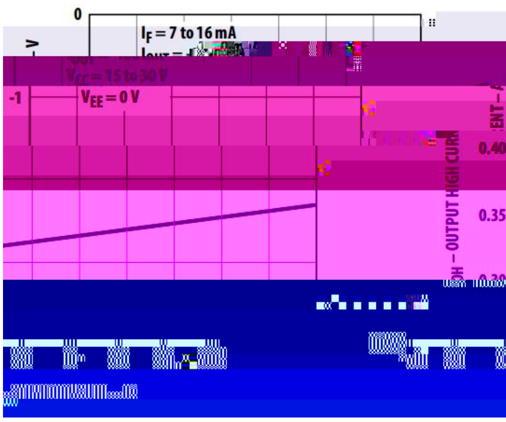


Figure 2: I_{OH} vs. Temperature

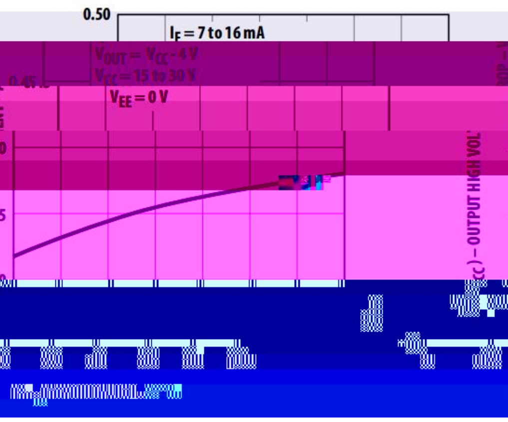


Figure 3: V_{OH} vs. I_{OH}

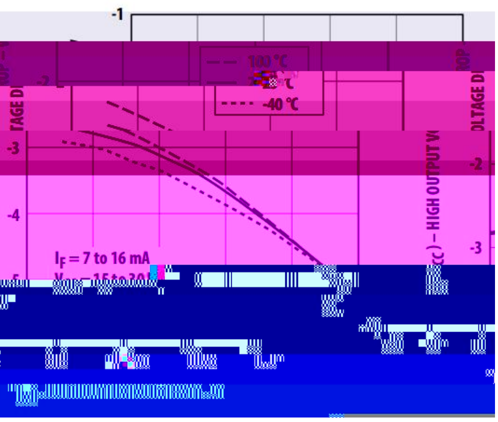


Figure 4: V_{OL} vs. Temperature

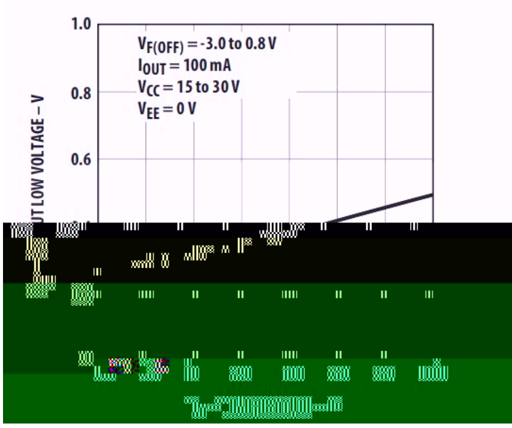


Figure 5: I_{OL} vs. Temperature

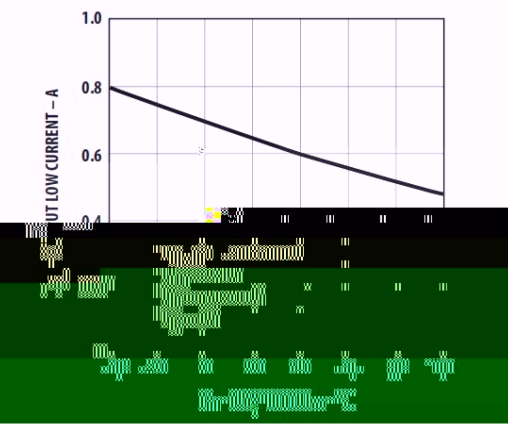


Figure 6: V_{OL} vs. I_{OL}

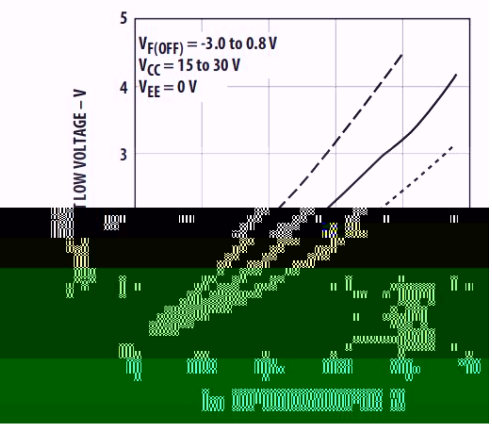


Figure 7: I_{CC} vs. Temperature

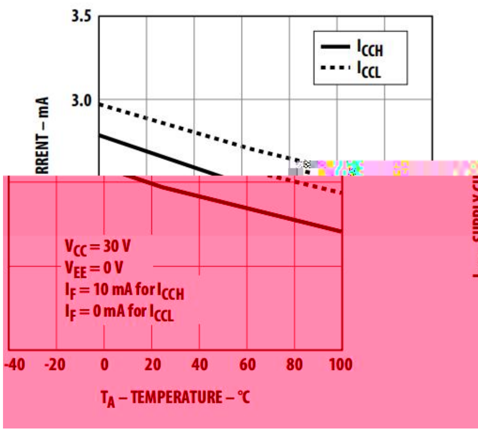


Figure 8: I_{CC} vs. V_{CC}

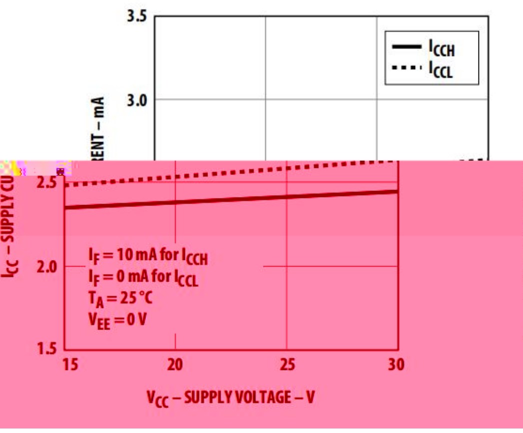


Figure 9: I_{FLH} vs. Temperature

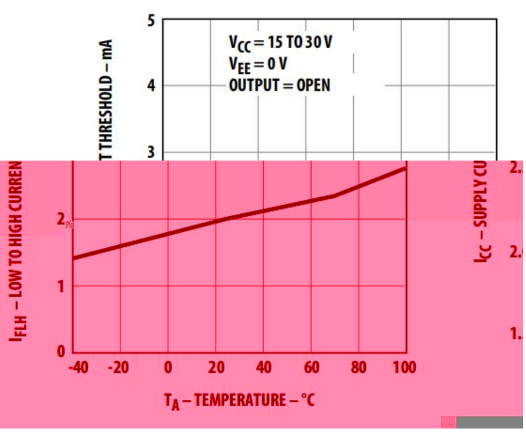


Figure 10 Propagation Delay vs. V_{CC} (OR-3120)

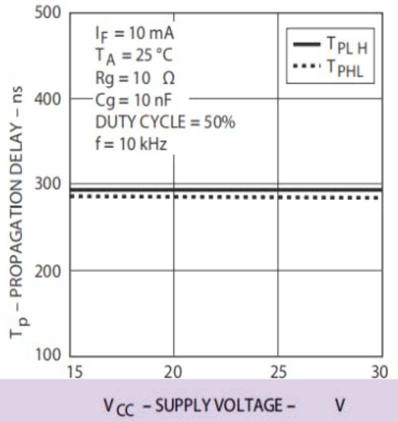


Figure 11 Propagation Delay vs. I_F (OR-3120)

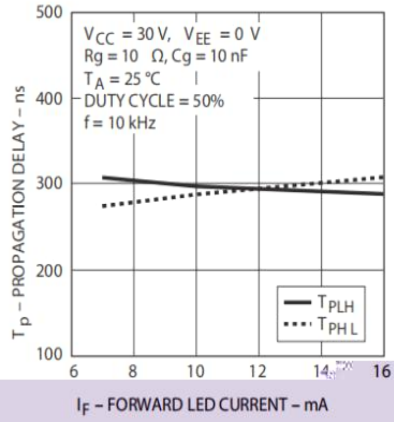
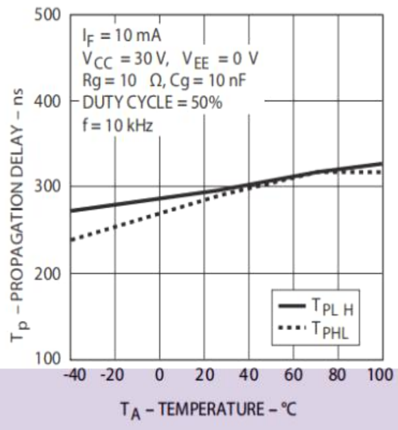
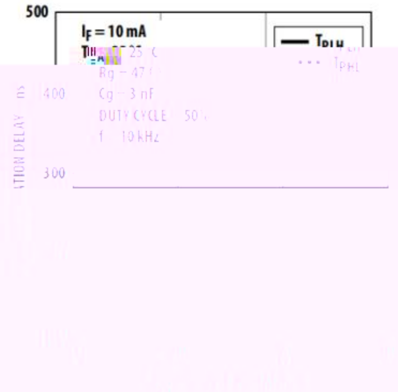


Figure 12 Propagation Delay vs. Temperature (OR-3120)



Propagation Delay vs. V_{CC} (OR-3150)



Propagation Delay vs. I_F (OR-3150)

Propagation Delay vs. Temperature (OR-3150)

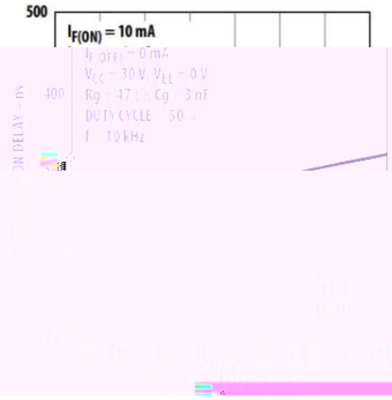
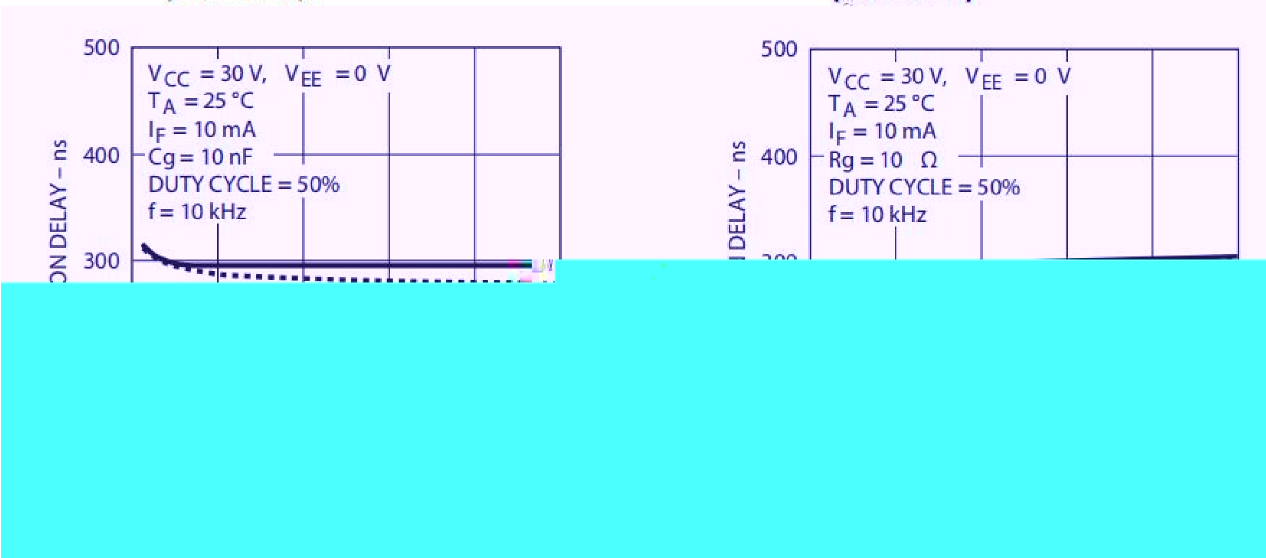


Figure 13 Propagation Delay vs. Rg (OR-3120) **Figure 14 Propagation Delay vs. Cg (OR-3120)**



Propagation Delay vs. Rg (OR-3150) **Propagation Delay vs. Cg (OR-3150)**

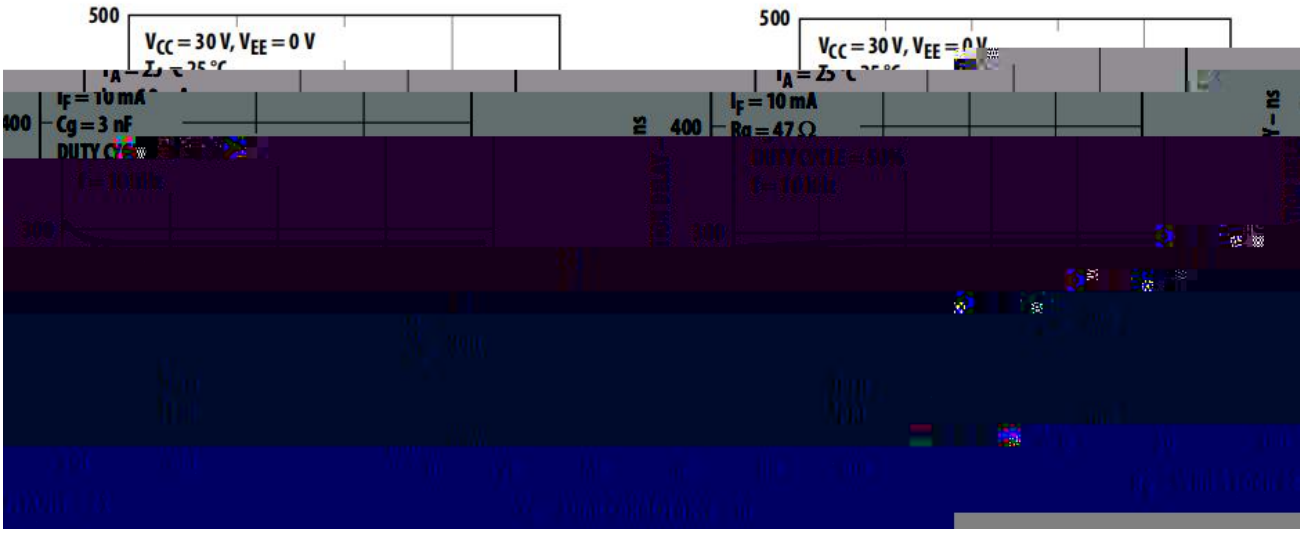


Figure 15 Transfer Characteristics

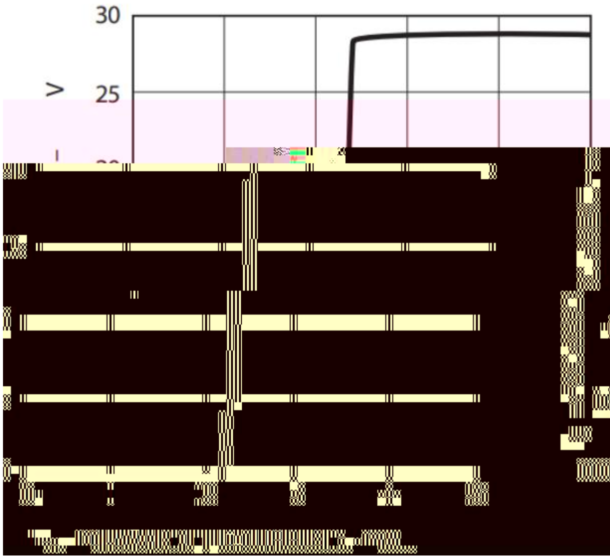


Figure 16 Input Current vs Forward Voltage

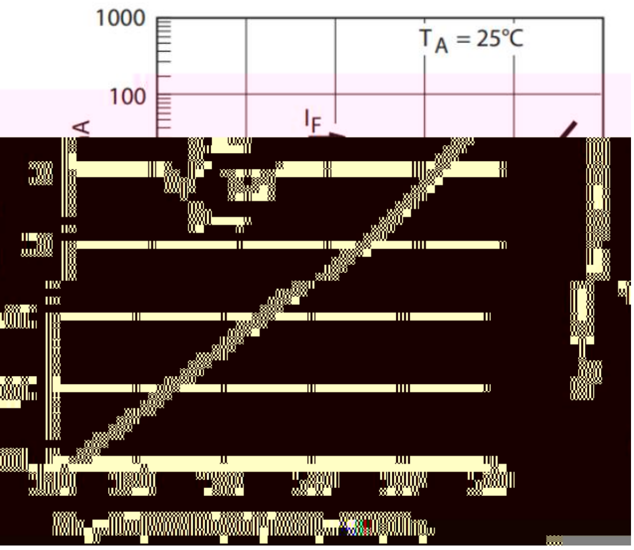


Figure 17：I$_{OH}$ Test Circuit

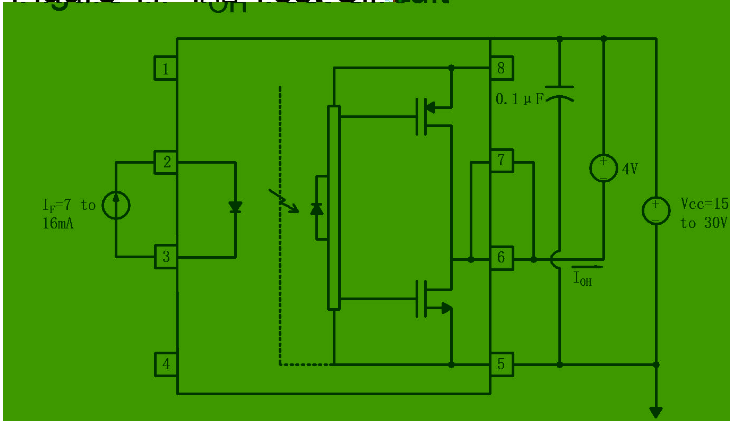


Figure 18：I$_{OL}$ Test Circuit

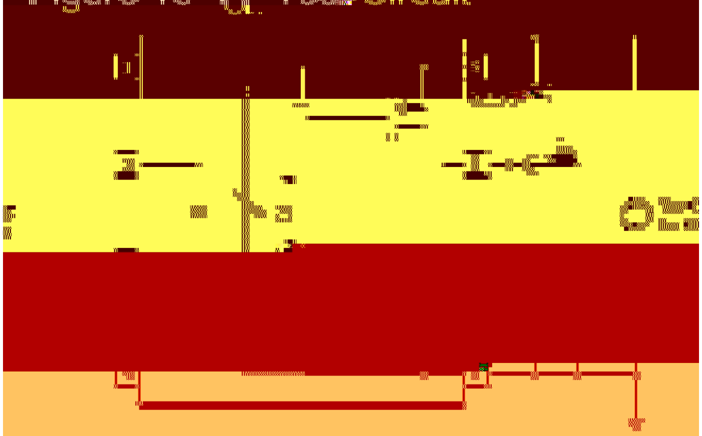


Figure 19：V$_{OH}$ Test Circuit

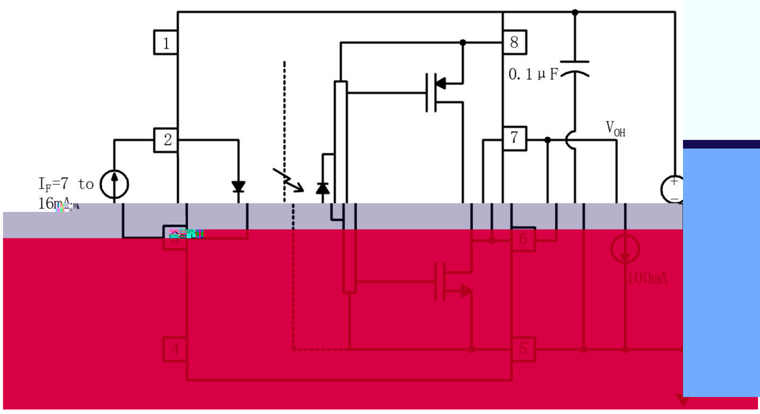


Figure 20：V$_{OL}$ Test Circuit

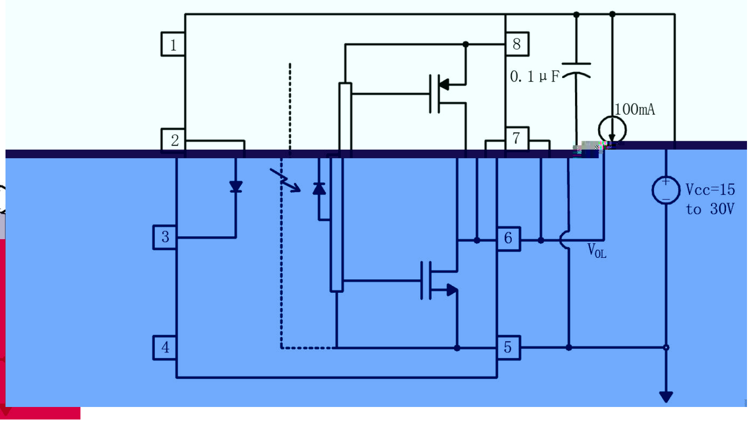


Figure 21 : I_{FLH} Test Circuit

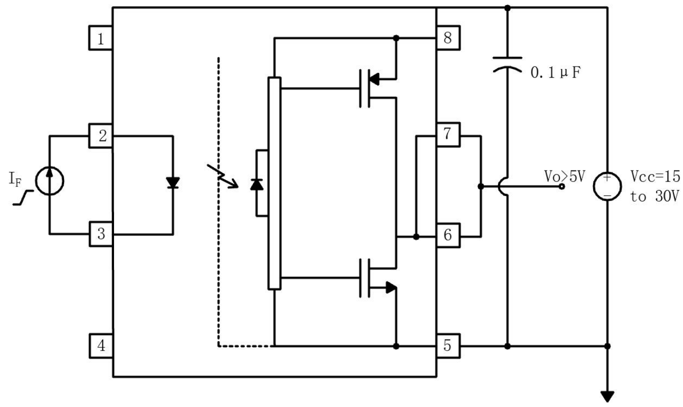


Figure 23: t_{PLH}, t_{PHL}, t_r, and t_f Test Circuit and Waveforms

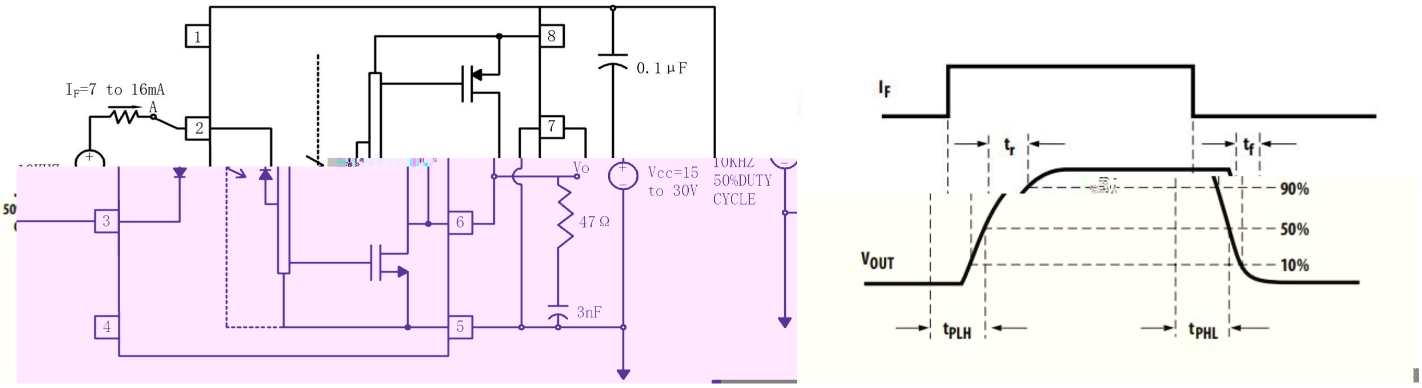


Figure 24: CMR Test Circuit and Waveforms